KIIT Deemed to be University
SPRING 2ND MID-SEMESTER EXAMINATION – 2017
DIGITAL ELECTRONICS (EC-2011)

Full Marks: 25   Duration: 1 hrs 30mins

- *Answer any 5 Questions and Q1 is compulsory.*
- *The figures in the margin indicate full marks.*
- *Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.*
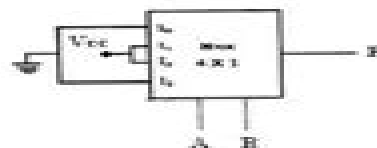
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1) a What are the drawbacks of 4-bit binary parallel adder circuit?   [1X5]

   b Define 'error detecting codes' and 'error correcting codes'.

   c Implement OR gate in a 2X1 MUX.

   d Draw a buffer gate using XNOR gate.

   e Draw a D-Flip-Flop using JK- Flip-Flop

2) Implement the following function using 8X1 MUX   [5]
$$F = \overline{A}B + \overline{C}D + \overline{A}C$$

3) Obtain the minimized expression using K.-map for the function   [5]
f=$\sum$m(0,1,2,3,8,9,10,11,14,15)+$\sum$d(6,7) and implement the minimized expression using NAND gates only

4) a Draw the logic diagram of full subtractor using minimum number of NAND gates.   [3]

   b Identify the Boolean function F(A,B) implemented with MUX   [2]

5) a Draw a 4-bit PISO Shift Register using D- Flip-Flop   [3]

   b What is Demultiplexer? How does it differ from a Decoder circuit   [2]

6) a Implement a Full-Adder in an active low decoder and using 2-input gates only.   [3]

   b What is BCD-SSD decoder? Also draw its truth table.   [2]

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