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Quantum Computer Systems

*Research for Noisy
Intermediate-Scale
Quantum Computers*

**Yongshan Ding
Frederic T. Chong**

***SYNTHESIS LECTURES ON
COMPUTER ARCHITECTURE***

Natalie Enright Jerger & Margaret Martonosi, Series Editors

Quantum Computing For Computer Architects Frederic T Chong

Daniel Sorin, Mark Hill, David Wood



Quantum Computing For Computer Architects Frederic T Chong:

Quantum Computing for Computer Architects Tzvetan S. Metodi, 2006 *Quantum Computing for Computer Architects* Tzvetan S. Metodi, Arvin I. Faruque, Frederic T. Chong, 2011 Quantum computation may seem to be a topic for science fiction but small quantum computers have existed for several years and larger machines are on the drawing table These efforts have been fueled by a tantalizing property while conventional computers employ a binary representation that allows computational power to scale linearly with resources at best quantum computations employ quantum phenomena that can interact to allow computational power that is exponential in the number of quantum bits in the system Quantum devices rely on the ability to control and manipulate binary data stored in the phase information of quantum wave functions that describe the electronic states of individual atoms or the polarization states of photons While existing quantum technologies are in their infancy we shall see that it is not too early to consider scalability and reliability In fact such considerations are a critical link in the development chain of viable device technologies capable of orchestrating reliable control of tens of millions quantum bits in a large scale system The goal of this lecture is to provide architectural abstractions common to potential technologies and explore the systems level challenges in achieving scalable fault tolerant quantum computation *Quantum Computing for Computer Architects, Second Edition* Tzvetan Metodi, Arvin I. Faruque, 2022-06-01 Quantum computers can in theory solve certain problems far faster than a classical computer running any known classical algorithm While existing technologies for building quantum computers are in their infancy it is not too early to consider their scalability and reliability in the context of the design of large scale quantum computers To architect such systems one must understand what it takes to design and model a balanced fault tolerant quantum computer architecture The goal of this lecture is to provide architectural abstractions for the design of a quantum computer and to explore the systems level challenges in achieving scalable fault tolerant quantum computation In this lecture we provide an engineering oriented introduction to quantum computation with an overview of the theory behind key quantum algorithms Next we look at architectural case studies based upon experimental data and future projections for quantum computation implemented using trapped ions While we focus here on architectures targeted for realization using trapped ions the techniques for quantum computer architecture design quantum fault tolerance and compilation described in this lecture are applicable to many other physical technologies that may be viable candidates for building a large scale quantum computing system We also discuss general issues involved with programming a quantum computer as well as a discussion of work on quantum architectures based on quantum teleportation Finally we consider some of the open issues remaining in the design of quantum computers Table of Contents Introduction Basic Elements for Quantum Computation Key Quantum Algorithms Building Reliable and Scalable Quantum Architectures Simulation of Quantum Computation Architectural Elements Case Study The Quantum Logic Array Architecture Programming the Quantum Architecture Using the QLA for Quantum Simulation The Transverse Ising Model Teleportation

Based Quantum Architectures Concluding Remarks

Quantum Computer Systems Yongshan Ding, Frederic T.

Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

Synthesis Lectures on Computer Architecture :

Quantum Computing for Computer Architects (2nd Edition) Tzvetan S. Metodi,

Deep Learning for Computer

Architects Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, David Brooks, 2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context

AI for Computer Architecture Lizhong Chen, Drew Penney, Daniel Jiménez, 2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system

wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs

Computer Architecture Techniques for Power-Efficiency Stefanos Kaxiras,Margaret Martonosi,2022-06-01 In the last few years power dissipation has become an important design constraint on par with performance in the design of new computer systems Whereas in the past the primary job of the computer architect was to translate improvements in operating frequency and transistor count into performance now power efficiency must be taken into account at every step of the design process While for some time architects have been successful in delivering 40% to 50% annual improvement in processor performance costs that were previously brushed aside eventually caught up The most critical of these costs is the inexorable increase in power dissipation and power density in processors Power dissipation issues have catalyzed new topic areas in computer architecture resulting in a substantial body of work on more power efficient architectures Power dissipation coupled with diminishing performance gains was also the main cause for the switch from single core to multi core architectures and a slowdown in frequency increase This book aims to document some of the most important architectural techniques that were invented proposed and applied to reduce both dynamic power and static power dissipation in processors and memory hierarchies A significant number of techniques have been proposed for a wide range of situations and this book synthesizes those techniques by focusing on their common characteristics Table of Contents Introduction Modeling Simulation and Measurement Using Voltage and Frequency Adjustments to Manage Dynamic Power Optimizing Capacitance and Switching Activity to Reduce Dynamic Power Managing Static Leakage Power Conclusions

Primer on Memory Consistency and Cache Coherence Daniel Sorin,Mark Hill,David Wood,2022-11-10 Many modern computer systems and most multicore chips chip multiprocessors support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both highlevel concepts as well as specific concrete examples from real world systems Table of Contents Preface Introduction to Consistency and Coherence Coherence Basics Memory Consistency Motivation and Sequential Consistency Total Store Order and the x86 Memory Model Relaxed Memory Consistency Coherence Protocols Snooping Coherence Protocols Directory

Coherence Protocols Advanced Topics in Coherence Author Biographies *On-Chip Photonic Interconnects* Christopher J. Nitta, Matthew Farrens, Venkatesh Akella, 2022-06-01 As the number of cores on a chip continues to climb architects will need to address both bandwidth and power consumption issues related to the interconnection network Electrical interconnects are not likely to scale well to a large number of processors for energy efficiency reasons and the problem is compounded by the fact that there is a fixed total power budget for a die dictated by the amount of heat that can be dissipated without special and expensive cooling and packaging techniques Thus there is a need to seek alternatives to electrical signaling for on chip interconnection applications Photonics which has a fundamentally different mechanism of signal propagation offers the potential to not only overcome the drawbacks of electrical signaling but also enable the architect to build energy efficient scalable systems The purpose of this book is to introduce computer architects to the possibilities and challenges of working with photons and designing on chip photonic interconnection networks Multi-Core Cache Hierarchies Rajeev

Balasubramonian, Norman Paul Jouppi, Naveen Muralimanohar, 2011 A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off chip memory consumes many more cycles and energy than on chip accesses In addition multi core processors are expected to place ever higher bandwidth demands on the memory system All these issues make it important to avoid off chip memory access by improving the efficiency of the on chip cache Future multi core processors will have many large cache banks connected by a network and shared by many cores Hence many important problems must be solved cache resources must be allocated across many cores data must be placed in cache banks that are near the accessing core and the most important data must be identified for retention Finally difficulties in scaling existing technologies require adapting to and exploiting new technology constraints The book attempts a synthesis of recent cache research that has focused on innovations for multi core processors It is an excellent starting point for early stage graduate students researchers and practitioners who wish to understand the landscape of recent cache research The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers Table of Contents Basic Elements of Large Cache Design Organizing Data in CMP Last Level Caches Policies Impacting Cache Hit Rates Interconnection Networks within Large Caches Technology Concluding Remarks

Introduction to Reconfigurable Supercomputing Marco Lanzagorta, Stephen Bique, Robert Rosenberg, 2022-05-31 This book covers technologies applications tools languages procedures advantages and disadvantages of reconfigurable supercomputing using Field Programmable Gate Arrays FPGAs The target audience is the community of users of High Performance Computers HPC who may benefit from porting their applications into a reconfigurable environment As such this book is intended to guide the HPC user through the many algorithmic considerations hardware alternatives usability issues programming languages and design tools that need to be understood before embarking on the creation of reconfigurable parallel codes We hope to show that FPGA acceleration based on the exploitation of the data parallelism pipelining and

concurrency remains promising in view of the diminishing improvements in traditional processor and system design Table of Contents FPGA Technology Reconfigurable Supercomputing Algorithmic Considerations FPGA Programming Languages Case Study Sorting Alternative Technologies and Concluding Remarks Phase Change Memory Naveen

Muralimanohar, Moinuddin K. Qureshi, Sudhanva Gurumurthi, Bipin Rajendran, 2022-05-31 As conventional memory technologies such as DRAM and Flash run into scaling challenges architects and system designers are forced to look at alternative technologies for building future computer systems This synthesis lecture begins by listing the requirements for a next generation memory technology and briefly surveys the landscape of novel non volatile memories Among these Phase Change Memory PCM is emerging as a leading contender and the authors discuss the material device and circuit advances underlying this exciting technology The lecture then describes architectural solutions to enable PCM for main memories Finally the authors explore the impact of such byte addressable non volatile memories on future storage and system designs Table of Contents Next Generation Memory Technologies Architecting PCM for Main Memories Tolerating Slow Writes in PCM Wear Leveling for Durability Wear Leveling Under Adversarial Settings Error Resilience in Phase Change Memories Storage and System Design With Emerging Non Volatile Memories **Efficient Processing of Deep Neural Networks**

Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel S. Emer, 2022-05-31 This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks DNNs DNNs are currently widely used for many artificial intelligence AI applications including computer vision speech recognition and robotics While DNNs deliver state of the art accuracy on many AI tasks it comes at the cost of high computational complexity Therefore techniques that enable efficient processing of deep neural networks to improve key metrics such as energy efficiency throughput and latency without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems The book includes background on DNN processing a description and taxonomy of hardware architectural approaches for designing DNN accelerators key metrics for evaluating and comparing different designs features of DNN processing that are amenable to hardware algorithm co design to improve energy efficiency and throughput and opportunities for applying new technologies Readers will find a structured introduction to the field as well as formalization and organization of key concepts from contemporary work that provide insights that may spark new ideas Automatic Parallelization Samuel

Midkiff, 2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss

some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading

Chip Multiprocessor Architecture Kunle Olukotun,Lance Hammond,James Laudon,2022-05-31 Chip multiprocessors also called multi core microprocessors or CMPs for short are now the only way to build high performance microprocessors for a variety of reasons Large uniprocessors are no longer scaling in performance because it is only possible to extract a limited amount of parallelism from a typical instruction stream using conventional superscalar instruction issue techniques In addition one cannot simply ratchet up the clock speed on today s processors or the power dissipation will become prohibitive in all but water cooled systems Compounding these problems is the simple fact that with the immense numbers of transistors available on today s microprocessor chips it is too costly to design and debug ever larger processors every year or two CMPs avoid these problems by filling up a processor die with multiple relatively simpler processor cores instead of just one huge core The exact size of a CMP s cores can vary from very simple pipelines to moderately complex superscalar processors but once a core has been selected the CMP s performance can easily scale across silicon process generations simply by stamping down more copies of the hard to design high speed processor core in each successive chip generation In addition parallel code execution obtained by spreading multiple threads of execution across the various cores can achieve significantly higher performance than would be possible using only a single core While parallel threads are already common in many useful workloads there are still important workloads that are hard to divide into parallel threads The low inter processor communication latency between the cores in a CMP helps make a much wider range of applications viable candidates for parallel execution than was possible with conventional multi chip multiprocessors nevertheless limited parallelism in key applications is the main factor limiting acceptance of CMPs in some types of systems After a discussion of the basic pros and cons of CMPs when they are compared with conventional uniprocessors this book examines how CMPs can best be designed to handle two radically different kinds of workloads that are likely to be used with a CMP highly parallel throughput sensitive applications at one end of the spectrum and less parallel latency sensitive applications at the other Throughput sensitive applications such as server workloads that handle many independent transactions at once require careful balancing of all parts of a CMP that can limit throughput such as the individual cores on chip cache memory and off chip memory interfaces Several studies and example systems such as the Sun Niagara that examine the necessary tradeoffs are presented here In contrast latency sensitive applications many desktop applications fall into this category require a focus on reducing inter core communication latency and applying techniques to help

programmers divide their programs into multiple threads as easily as possible This book discusses many techniques that can be used in CMPs to simplify parallel programming with an emphasis on research directions proposed at Stanford University To illustrate the advantages possible with a CMP using a couple of solid examples extra focus is given to thread level speculation TLS a way to automatically break up nominally sequential applications into parallel threads on a CMP and transactional memory This model can greatly simplify manual parallel programming by using hardware instead of conventional software locks to enforce atomic code execution of blocks of instructions a technique that makes parallel coding much less error prone Contents The Case for CMPs Improving Throughput Improving Latency Automatically Improving Latency using Manual Parallel Programming A Multicore World The Future of CMPs **Performance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU)** Hyesoon Kim, Richard Vuduc, Sara Baghsorkhi, Jee Choi, Wen-mei W. Hwu, 2022-05-31 General purpose graphics processing units GPGPU have emerged as an important class of shared memory parallel processing architectures with widespread deployment in every computer class from high end supercomputers to embedded mobile platforms Relative to more traditional multicore systems of today GPGPUs have distinctly higher degrees of hardware multithreading hundreds of hardware thread contexts vs tens a return to wide vector units several tens vs 1 10 memory architectures that deliver higher peak memory bandwidth hundreds of gigabytes per second vs tens and smaller caches scratchpad memories less than 1 megabyte vs 1 10 megabytes In this book we provide a high level overview of current GPGPU architectures and programming models We review the principles that are used in previous shared memory parallel platforms focusing on recent results in both the theory and practice of parallel algorithms and suggest a connection to GPGPU platforms We aim to provide hints to architects about understanding algorithm aspect to GPGPU We also provide detailed performance analysis and guide optimizations from high level algorithms to low level instruction level optimizations As a case study we use n body particle simulations known as the fast multipole method FMM as an example We also briefly survey the state of the art in GPU performance analysis tools and techniques Table of Contents GPU Design Programming and Trends Performance Principles From Principles to Practice Analysis and Tuning Using Detailed Performance Analysis to Guide Optimization **Shared-Memory Synchronization** Michael L. Scott, 2022-05-31 This book offers a comprehensive survey of shared memory synchronization with an emphasis on systems level issues It includes sufficient coverage of architectural details to understand correctness and performance on modern multicore machines and sufficient coverage of higher level issues to understand how synchronization is embedded in modern programming languages The primary intended audience for this book is systems programmers the authors of operating systems library packages language run time systems concurrent data structures and server and utility programs Much of the discussion should also be of interest to application programmers who want to make good use of the synchronization mechanisms available to them and to computer architects who want to understand the ramifications of their design decisions

on systems level code **Compiling Algorithms for Heterogeneous Systems** Steven Bell, Jing Pu, James Hegarty, Mark Horowitz, 2022-05-31 Most emerging applications in imaging and machine learning must perform immense amounts of computation while holding to strict limits on energy and power To meet these goals architects are building increasingly specialized compute engines tailored for these specific tasks The resulting computer systems are heterogeneous containing multiple processing cores with wildly different execution models Unfortunately the cost of producing this specialized hardware and the software to control it is astronomical Moreover the task of porting algorithms to these heterogeneous machines typically requires that the algorithm be partitioned across the machine and rewritten for each specific architecture which is time consuming and prone to error Over the last several years the authors have approached this problem using domain specific languages DSLs high level programming languages customized for specific domains such as database manipulation machine learning or image processing By giving up generality these languages are able to provide high level abstractions to the developer while producing high performance output The purpose of this book is to spur the adoption and the creation of domain specific languages especially for the task of creating hardware designs In the first chapter a short historical journey explains the forces driving computer architecture today Chapter 2 describes the various methods for producing designs for accelerators outlining the push for more abstraction and the tools that enable designers to work at a higher conceptual level From there Chapter 3 provides a brief introduction to image processing algorithms and hardware design patterns for implementing them Chapters 4 and 5 describe and compare Darkroom and Halide two domain specific languages created for image processing that produce high performance designs for both FPGAs and CPUs from the same source code enabling rapid design cycles and quick porting of algorithms The final section describes how the DSL approach also simplifies the problem of interfacing between application code and the accelerator by generating the driver stack in addition to the accelerator configuration This book should serve as a useful introduction to domain specialized computing for computer architecture students and as a primer on domain specific languages and image processing hardware for those with more experience in the field *Deep Learning Systems* Andres Rodriguez, 2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models

and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to better collaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book

This book delves into Quantum Computing For Computer Architects Frederic T Chong. Quantum Computing For Computer Architects Frederic T Chong is a crucial topic that must be grasped by everyone, from students and scholars to the general public. This book will furnish comprehensive and in-depth insights into Quantum Computing For Computer Architects Frederic T Chong, encompassing both the fundamentals and more intricate discussions.

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