

# Simulating Verilog RTL using Synopsys VCS

6.375 Tutorial 1  
February 1, 2008

In this tutorial you will gain experience using Synopsys VCS to compile cycle-accurate executable simulators from Verilog RTL. You will also learn how to use the Synopsys Waveform viewer to trace the various signals in your design. Figure 1 illustrates the basic VCS and SMIPS assembler toolflow. VCS takes a set of Verilog files as input and produces a simulator. When we execute the simulator we need some way to observe our design so that we can measure its performance and verify that it is working correctly. There are two primary ways to observe our design: (1) we can use `$display` statements in our Verilog RTL to output textual trace information, or (2) we can instruct the simulator to automatically write transition information about each signal in our design to a file. There is standard text format for this type of signal transition trace information called the Value Change Dump format (VCD). Unfortunately, these textual trace files can become very large very quickly, so Synopsys uses a proprietary compressed binary trace format called VCD Plus (VPD). We can view VPD files using the Synopsys waveform viewer called VirSim.

We will be using a simple unpipelined SMIPSV1 processor as our design example for this tutorial, and thus you will also learn the how to build and run test codes on the processor simulator. Figure 2 shows the block diagram for the example processor. Figure 1 shows the SMIPS assembler toolflow which starts with an SMIPS assembly file and uses several tools to generate a Verilog Memory Hex (VMH) file suitable to run on the cycle-accurate simulator. This tutorial assumes you are familiar with the SMIPS ISA. For more information please consult the *SMIPS Processor Specification*.

For more information consult the CVS user manual ([cvs-user-guide.pdf](#)) located in the course locker ([/mit/6.375/doc](#)).

## Getting started

Before using the 6.375 toolflow you must add the course locker and run the course setup script with the following two commands.

```
% add 6.375
% source /mit/6.375/setup.csh
```

# Vcs Getting Started Guide

**Cifor**



## Vcs Getting Started Guide:

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**Effective guide for GitLab migration from GitHub and SVN**

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Set up CI and test builds for your projects

Understand the benefits and limitations of GitLab workflow

Migrate from other common VCS platforms to Gitlab

Create review and merge code changes

Learn to branch local code and create a new branch in GitLab

Configure sequential stages and simultaneous stages for CI

CD Access Mattermost for on premise GitLab

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## Table of Contents Vcs Getting Started Guide

1. Understanding the eBook Vcs Getting Started Guide
  - The Rise of Digital Reading Vcs Getting Started Guide
  - Advantages of eBooks Over Traditional Books
2. Identifying Vcs Getting Started Guide
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Vcs Getting Started Guide
  - User-Friendly Interface
4. Exploring eBook Recommendations from Vcs Getting Started Guide
  - Personalized Recommendations
  - Vcs Getting Started Guide User Reviews and Ratings
  - Vcs Getting Started Guide and Bestseller Lists
5. Accessing Vcs Getting Started Guide Free and Paid eBooks
  - Vcs Getting Started Guide Public Domain eBooks
  - Vcs Getting Started Guide eBook Subscription Services
  - Vcs Getting Started Guide Budget-Friendly Options
6. Navigating Vcs Getting Started Guide eBook Formats
  - ePub, PDF, MOBI, and More
  - Vcs Getting Started Guide Compatibility with Devices
  - Vcs Getting Started Guide Enhanced eBook Features
7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Vcs Getting Started Guide
  - Highlighting and Note-Taking Vcs Getting Started Guide
  - Interactive Elements Vcs Getting Started Guide
8. Staying Engaged with Vcs Getting Started Guide

- Joining Online Reading Communities
- Participating in Virtual Book Clubs
- Following Authors and Publishers Vcs Getting Started Guide
- 9. Balancing eBooks and Physical Books Vcs Getting Started Guide
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Vcs Getting Started Guide
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Vcs Getting Started Guide
  - Setting Reading Goals Vcs Getting Started Guide
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Vcs Getting Started Guide
  - Fact-Checking eBook Content of Vcs Getting Started Guide
  - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
- 14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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