



FEDERAL PUBLIC SERVICE COMMISSION
COMPETITIVE EXAMINATION-2021 FOR RECRUITMENT TO
POSTS IN BS-17 UNDER THE FEDERAL GOVERNMENT
COMPUTER SCIENCE, PAPER-II

Roll Number

TIME ALLOWED: THREE HOURS	PART-I (MCQS)	MAXIMUM MARKS = 20
PART-I(MCQS): MAXIMUM 30 MINUTES	PART-II	MAXIMUM MARKS = 80

NOTE: (i) Part-II is to be attempted on the separate Answer Book.
(ii) Attempt **ONLY FOUR** questions from **PART-II** by selecting **TWO** questions from **EACH SECTION**. **ALL** questions carry **EQUAL** marks.
(iii) All the parts (if any) of each Question must be attempted at one place instead of at different places.
(iv) Candidate must write Q. No. in the Answer Book in accordance with Q. No. in the Q.Paper.
(v) No Page/Space be left blank between the answers. All the blank pages of Answer Book must be crossed.
(vi) Extra attempt of any question or any part of the attempted question will not be considered.

PART – II (SECTION – A)

- Q. 2.**
- The addressing in a typical instruction format are done by using different addressing modes. Examine any five addressing modes with an example based on the contents of address field, actual address and contents of memory location. (10)
 - The decimal value of address field in an instruction is 120. The addressing mode of the machine's architecture is register direct and register indirect addressing. Calculate the address of corresponding operand. (5)
 - Compare the set of addressing modes of RISC and CISC machines. Give one example of addressing modes used in RISC and CISC respectively. (5)

- Q. 3.** Memory managed by BITMAP is shown below:

1	1	1	1	1	0
0	1	1	0	0	0
1	0	0	1	1	1
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	1

- Show properly filled memory according to the BITMAP where memory index starts from zero. (3)
- Insert a page H of size 3 allocation units in memory drawn in part 'a' using first-fit algorithm. Redraw memory and the BITMAP after insertion. (3)
- Now insert another page K of size 2 allocation units in memory drawn in part 'b' using next-fit algorithm. Redraw memory and the BITMAP after insertion. (3)
- Use linked list data structure for the above memory mapping (Only give equivalent figure). (6)
- Use hash table to keep track of active pages in the above memory (Only give figure). (5)

- Q. 4.** Do as directed:

- Calculate effective memory access time using following data: (3)
 - TLB hit ratio is 85%.
 - TLB access time=20nsec
 - Memory access time=115nsec

Effective memory access time = Hit rate * (TLB access time + Mem access time) + (1 - Hit rate) * (TLB access time + Process table access time + Mem access time)

- Consider a logical address and physical address of 31 and 22 bits respectively. What will be total logical and physical address space? (4)
- Does resource allocation graph shown below consist of a deadlock or not? Justify with reason. (3)



(Figure: Resource Allocation Graph)

- What is race condition? What are the different techniques to avoid race condition in the processes? Which one is optimal and why? (10)

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