

Automatic Verilog Code Generation through Grammatical Evolution

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ABSTRACT

This work aims to investigate the automatic generation of Verilog code, representing digital circuits through Grammatical Evolution (GE). Preliminary tests using a simple full adder generation problem have been performed.

Categories and Subject Descriptors

I.2.2 [Artificial Intelligence]: Automatic Programming – program synthesis, program verification.

General Terms

Design, Verification.

Keywords

Grammatical Evolution, Automatic Code Generation, Verilog.

1. INTRODUCTION

Application of a HDL (Hardware Description Language) represents a basic step in the ASIC (Application Specific Integrated Circuit) design flow. In this context, (mostly) a digital circuit is represented in Verilog or VHDL. Then simulations are performed to check the functionality of the generated circuit representation. If the circuit model generated by a HDL shows the expected behavior, synthesis of the circuit, the conversion of the HDL code to an ensemble of logic gates, follows [2]. Because the syntax of Verilog is simpler, Verilog-code generation is aimed for in this study.

In Verilog, circuits can be described at various abstraction levels: behavioral, structural and RTL (Register Transfer Level) coding [4]. Behavioral coding provides a “black box” representation of the circuit to be designed and cannot be synthesized. Structural coding reflects components of a design (e. g. logic gates) and interconnections between them. RTL coding, representing the functionality of a design at register transfer level, employs only the synthesizable portion of Verilog syntax. The most descriptive type is behavioral, then RTL, and finally structural coding [2].

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Generation of synthesizable Verilog code, using RTL coding, is intended within the scope of this work. Circuit models generated by synthesis tools stand in strong correlation with the HDL code written to represent the functionality of the circuit to be designed [2]. Automatic Verilog code generation through Grammatical Evolution covers this step.

2. DETERMINATION OF THE EVOLUTIONARY TECHNIQUE SUITED TO VERILOG CODE GENERATION

2.1 Genetic Programming (GP)

The first technique considered was Genetic Programming (GP). Since each element in the solution space of the problem is depicted as a tree, GP provides a proper representation mechanism for the automatic code¹ generation paradigm [1]. Main limitation of GP over crossover and mutation is closure. Closure allows any two points in a tree representing a computer program to be crossed over without loss of validity [11]. The set of syntactically valid individuals should be closed over the genetic operations. To achieve this, each non-terminal node of the tree representation of a program is expected to have the same arity and a return value of the same type [10].

Verilog syntax permits the use of code blocks such as “if” and “always”, which should be protected against the destructive operation of crossover. GP’s modularization scheme, Automatically Defined Functions (ADFs) can be used to achieve this. Besides, Verilog syntax constraints include:

1. An input variable on the left hand side of an assignment is not allowed.
2. An assignment cannot be generated as the condition statement of an “if” or “always” block.
3. Depending on the nature of the circuit to be represented, zero or more “always” blocks or alternatively zero or more assignment statements should be brought together. For instance, an expression defining the right hand side of an assignment, or a conditional statement (expected to be used in the context of an “if” or “always” block) should not be generated without context to represent a line of code.

If standard GP is used, the set of non-terminals consist of Verilog operators. To define constraint 1, e. g., the left child of a subtree having an assignment operator in its root should be restricted to include an element from the set of output variables, while various logical, bitwise, reduction or concatenation operators can be placed at the right hand side child. As no rules can be defined to

¹ In this work, “code” is used to specify Verilog code.

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